RF Measurements and Characterization of Heterostructure Field-Effect Transistors at Low Temperatures

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Abstract—**The RF performance of both conventional AlGaAs/GaAs and superlattice AlAs/GaAs heterostructure field-effect transistors has been investigated at 120 K and the results are compared with room-temperature values. Both the system used for low-temperature RF measurements up to 12 GHz and the procedure to extract the equivalent circuit from measured *S* parameters of the packaged FET are described. The high-frequency performance of the HFET's is strongly improved at low temperatures but is sensitive to light due to the device structure. Both the problems of low-temperature measurements and the results of the RF investigation are discussed.**

I. INTRODUCTION

DUE TO ENHANCED transport properties at low temperatures, improved performance of AlGaAs/GaAs heterostructure field-effect transistors (HFET's) compared to GaAs MESFET's is expected. Numerous publications demonstrate the applicability and advantages of these structures at room temperature [1]–[3]. HFET's optimized for microwave applications show higher transconductances and gain and lower noise figures than MESFET's [4]–[6]. The main advantage of heterostructures is the pronounced mobility enhancement at low temperatures, from which fact an improved dc and RF performance can be expected [7], [8]. The parasitic resistances as well as the channel noise will be strongly reduced [9].

Nowadays RF performance at room temperature is usually measured by using a wafer-probing system. The FET can be directly characterized in this temperature range. But investigations at low temperatures are not possible by this means. Therefore a new measurement system based on a conventional HP network analyzer was developed for RF characterization at 120 K up to 12 GHz. This system as well as the investigated devices will be described in the first part of this paper. The FET's have to be bonded and packaged for measurements into a conventional transistor test fixture (TTF). But parasitic inductances and capacitances may no longer be neglected. Therefore it is necessary to extract the intrinsic FET parameters from the measured scattering parameters by determination of an exact equivalent circuit. The method which was used for this work is described in this paper. Problems with low-temperature measurements and the influence of the package will be analyzed in detail. The results of the low-temperature investigations are presented in the second part of this paper. The dependences of the elements of the equivalent circuit as well as the gain on temperature and illumination will be investigated and discussed.

II. RF MEASUREMENT SETUP

To characterize the low-temperature RF performance of heterostructure FET's, the existing *S*-parameter measurement setup based on a network analyzer (HP8510) had to be modified. The samples are bonded into customary industrial packages and measured in a commercial transistor test fixture (HP85041). This fixture consists of three components: two outer ones, which include the RF connectors (APC7), and the middle part, which takes up the device. The last one was replaced by a new construction which includes a silicon pn diode for measuring the actual temperature (Fig. 1). Additionally a red LED was integrated face to face to the device under test to investigate the light dependence of the high-frequency performance at low temperatures. This is very important for heterostructures, as will be shown in Section V. The modified TTF is affixed to the cold head at the bottom of a nitrogen cryostat in an evacuated chamber (Fig. 2). The fixture is connected by RF cables with a high thermal resistance to avoid freezing of the connectors outside the vacuum cham-

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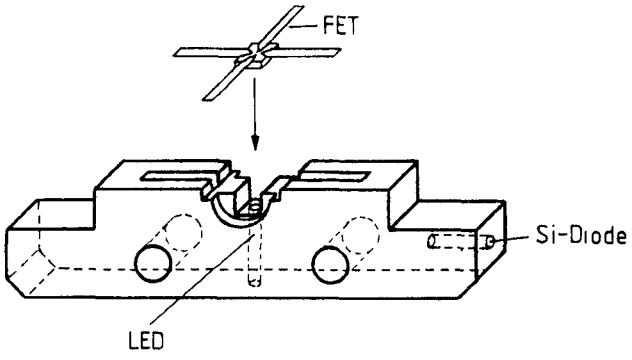


Fig. 1. Modified part of the commercial transistor test fixture (TTF) with a LED for illumination and a pn diode for temperature measurement.

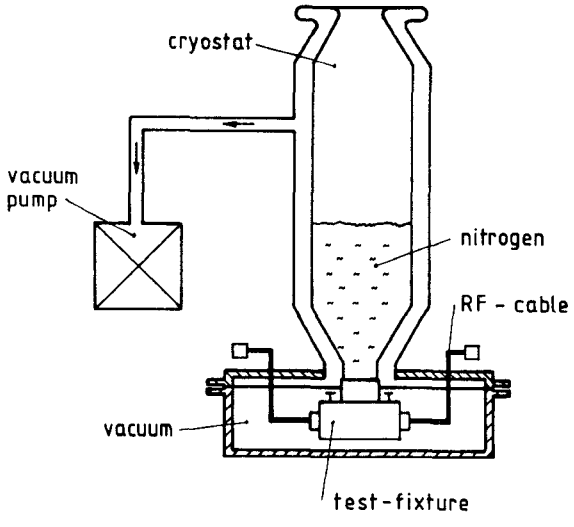


Fig. 2. Setup for low-temperature RF measurements.

ber and to achieve a lower temperature. The lowest temperature which can be achieved in the test fixture is about 120 K. The scattering parameters can be measured up to 12 GHz. The measurement setup is conventionally calibrated at room temperature by a short, an open, and a sliding load. The change of the reference plane due to the shortening of the electrical lengths of cables and connectors caused by the temperature reduction is considered by a correction of the phase shift. During measurement the influence of the test fixture is taken into account by the original HP de-embedding software. Remaining parasitics of the package are considered by additional elements in the equivalent circuit which is determined from measured S parameters.

III. Device Preparation and DC Performance

The reason for developing a system for low-temperature RF measurements is the strong temperature dependence of heterostructure FET performance. While low-field mobility in heterostructures rises and parasitic resistances decrease by lowering the temperature, the conventional AlGaAs/GaAs HFET's (Fig. 3(a)) exhibit the well-known collapse of the $I-V$ characteristics and a strong threshold voltage shift [10]. Illumination of the devices avoids these

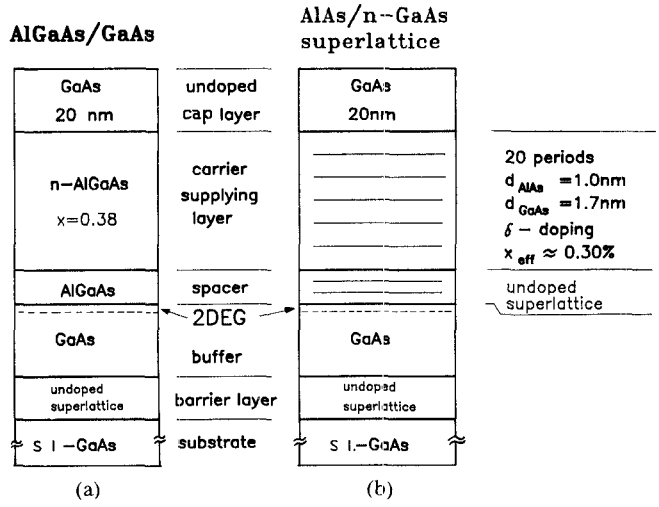
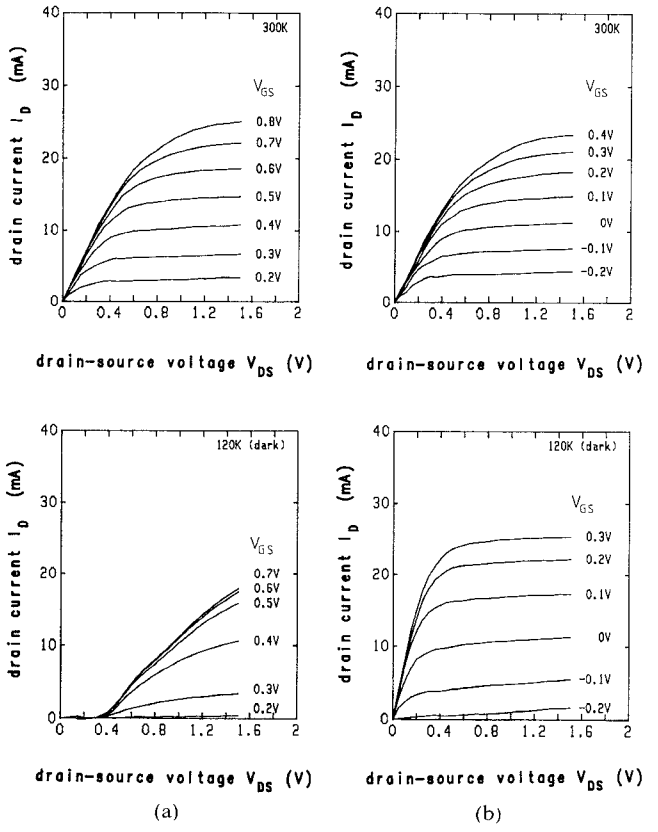


Fig. 3. Structure of the investigated heterostructure FET's: (a) conventional n-AlGaAs/GaAs HFET; (b) AlAs/GaAs superlattice HFET.

negative effects, and the expected increase in transconductance can be measured [11]. The low-temperature performance is affected by the behavior of the doped n-$Al_xGa_{1-x}As$ layer. The activation energy of donors incorporated is shallow insofar as the Al content and the doping level are low [12]. But both the Al content ($x > 25$ percent) and the doping concentration ($> 5 \cdot 10^{17}$ cm^{-3}) have to be high to obtain layers with a high two-dimensional electron gas (2DEG) concentration and a good confinement suitable for microwave applications [13]. Under these conditions a large number of donors become deep (DX-center), resulting in freeze-out of carriers, $I-V$ collapse, and persistent photoconductivity at low temperatures. Replacing the doped n-AlGaAs layer with a n-GaAs/AlAs superlattice (Fig. 3(b)) reduces these low-temperature effects [14], [15].

Structures of both types were grown by MBE in a Varian Gen II system. The growth rate was approximately 1 μm/h with a conventional As_4 source. The substrate temperature for both types was 620°C. Onto a semi-insulating 100-oriented GaAs substrate a barrier superlattice consisting of four GaAs wells sandwiched between five AlGaAs wells was grown to suppress the influence of substrate effects on the device performance. This superlattice is followed by a 1 μm p$^-$-GaAs buffer with the 2DEG near the spacer layer. In the case of the conventional structure the spacer is realized by an undoped $Al_xGa_{1-x}As$ layer followed by the n-$Al_xGa_{1-x}As$ as carrier-supplying layer. Various HFET's were measured, with comparable results. Therefore in this paper only the representative results of one conventional and one superlattice HFET are presented.

In the n-GaAs/AlAs superlattice structure the undoped AlGaAs spacer layer is replaced by two 1.7 nm GaAs wells sandwiched between three 1.0 nm AlAs barriers. In order to spatially separate the dopant from the aluminum in the carrier-supplying layer the n-$Al_xGa_{1-x}As$ layer above the spacer in the conventional structure is replaced by a 20 period superlattice of 1.7 nm GaAs wells and 1.0 nm AlAs



(a) (b)

Fig. 4. DC characteristic of (a) conventional n-AlGaAs/GaAs HFET and (b) superlattice AlAs/GaAs HFET at 300 K and at 120 K in the dark.

barriers. The doping in the superlattice is performed as a spike doping in each GaAs well. The effective Al content of this structure is about 30 percent. The thicknesses of the undoped and doped superlattices are 6 nm and 54 nm, respectively. On top of both structures an undoped 20 nm GaAs cap layer was grown. The thicknesses of the spacer and the n-AlGaAs layer are 6 nm and 50 nm, respectively. This superlattice structure combines the advantage of a high Al content to improve the confinement of carriers in the 2DEG and consequently the room-temperature operation but exhibits no degradation effects at low temperatures (Fig. 4).

The growth parameters were chosen such that the fabricated devices are comparable concerning their effective Al content and effective doping concentration at room temperature. The incorporated doping density in both carrier-supplying layers is $2 \cdot 10^{13}\ \mathrm{cm}^{-2}$, resulting in a sheet carrier concentration in the 2DEG of only $1 \cdot 10^{12}\ \mathrm{cm}^{-2}$. Since the two structures are not completely identical, it is necessary to compare the relative change of the device characteristics at low temperatures, but not the absolute values. In both cases the gate length of the fabricated HFET's is 1.5 μm with a drain–source spacing of 5 μm and a gate–source distance of 1.5 μm. The total width of the gate consisting of two fingers is 300 μm. The gate is recessed by wet chemical etching. For low-temperature RF measurements the devices have to be bonded and packaged. Although the devices had fairly long gates it may be anticipated that the performance of conventional and superlattice HFET's with submicron gates at low temperatures and under illumination will show the same general behavior. Thus the conclusions to be drawn here can be transferred to submicron devices.

IV. Determination of Equivalent Circuit and Influence of Parasitic Elements

When measuring packaged devices the influence of parasitic inductances and capacitances cannot be neglected. Therefore it is necessary to determine a complete equivalent circuit including parasitics to evaluate the intrinsic FET. Different methods are known in the literature, some of which were tested for this work and modified where necessary. The method based on [16] is a numerical optimization procedure to find the minimal difference between measured parameters and calculated parameters from the equivalent circuit. However a solution relevant to the physical correlation of the device is not always warranted. To improve the reliability the method based on [17] consists of three steps. First, parasitic resistances are determined by dc measurements. Then the parasitic capacitances and inductances are extracted from S parameters of the FET measured without bias voltage and a simplified equivalent circuit is determined. Finally the remaining elements are optimized from the S parameters obtained at each bias point. This method is very time consuming. If parasitics have a negligible effect on the measurement most elements can be determined from the parameters measured at low frequencies (up to 5 GHz) by a step by step optimization as published in [18].

If a transistor package is used, these negative influences cannot be neglected and the influence can be described by additional capacitances C_{in}, C_{out} and inductances. To determine all the elements the method outlined in [19] was modified. At first a sensitivity analysis is done to decide how the different elements affect the various S parameters. For this method the influence of each element on the different scattering parameters is investigated by successively varying one element after another while keeping all the other elements constant. Then one S parameter of the equivalent circuit after another is fitted to the measured parameters, varying only as many as three elements at the same time. Table I shows the sequence of S-parameter optimization and the corresponding elements which are taken into account for each step. This sequence differs from the one proposed in [19] due to the results of the described sensitivity analysis. This step is repeated until a minimal difference between measured and calculated parameters is achieved. The optimization procedure for determining the elements is combined with the method outlined in [16]. With the help of this modified procedure the equivalent circuit of a conventional HFET at 120 K was determined (Fig. 5). The calculated parasitics are $C_{in} = 0.11$ pF, $C_{out} = 0.1$ pF, $L_G = 0.57$ nH, $L_S = 0.09$ nH, and $L_D = 0.35$ nH, which are typical values for the investigated FET's. RF measurements of various packaged devices result in almost the same values. Fig. 6 demonstrates the

TABLE I
SEQUENCE USED FOR OPTIMIZATION OF *S* PARAMETERS

Step	Element	*S* Parameter
1	C_{gs}, R_{gs}	S_{11}
2	C_d, R_d	S_{22}
3	C_{gd}, R_s	S_{12}
4	g_m, τ	S_{21}
5	L_G, R_G, C_{in}	S_{11}
6	L_D, R_D, C_{out}	S_{22}
7	L_s	S_{12}
8	g_m, τ	S_{21}

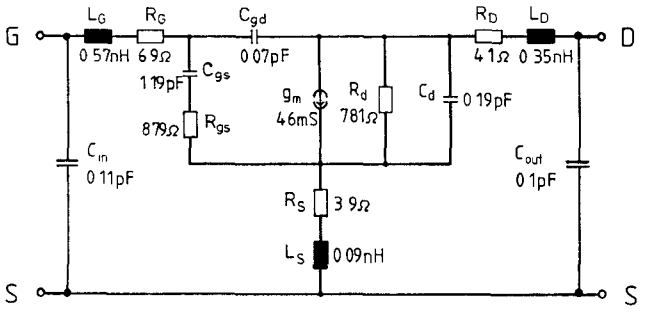


Fig. 5. Equivalent circuit of the AlGaAs/GaAs HFET for $V_{DS} = 2.5$ V and $V_{GS} = 0.3$ V, calculated from *S* parameters in Fig. 6.

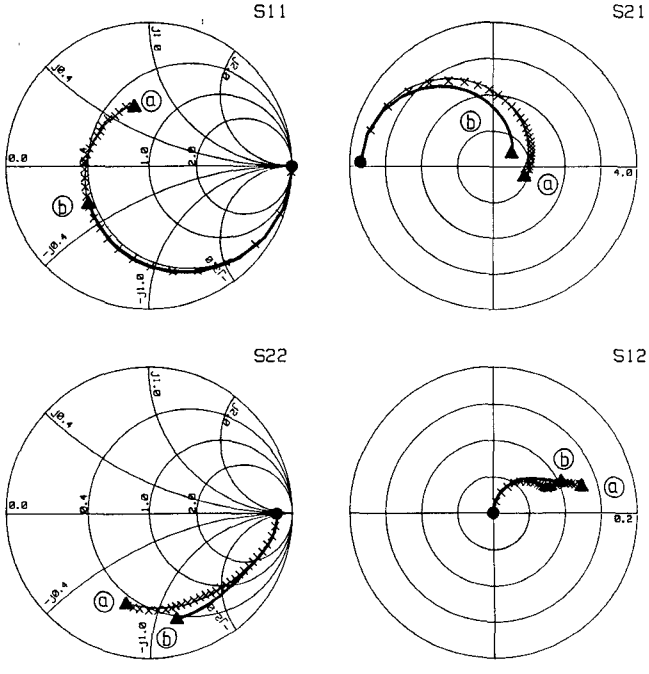


Fig. 6. Curve *a*: comparison of *S* parameters measured (×) and from equivalent circuit in Fig. 4 calculated (−). Curve *b*: *S* parameters calculated from equivalent circuit in Fig. 5 without consideration of $C_{in}, C_{out}, L_G, L_S, L_D$ (∘: 45 MHz, Δ: 10 GHz).

reliability and the good agreement between measured and calculated *S* parameters (curve *a*).

The inductances determined from *S* parameters measured by use of a wafer prober are only about 0.05 nH. In this case no remarkable parasitic capacitances influence the results. This means the determined parasitics are caused only by the transistor package. To investigate how this package affects the RF measurements, the *S* parameters

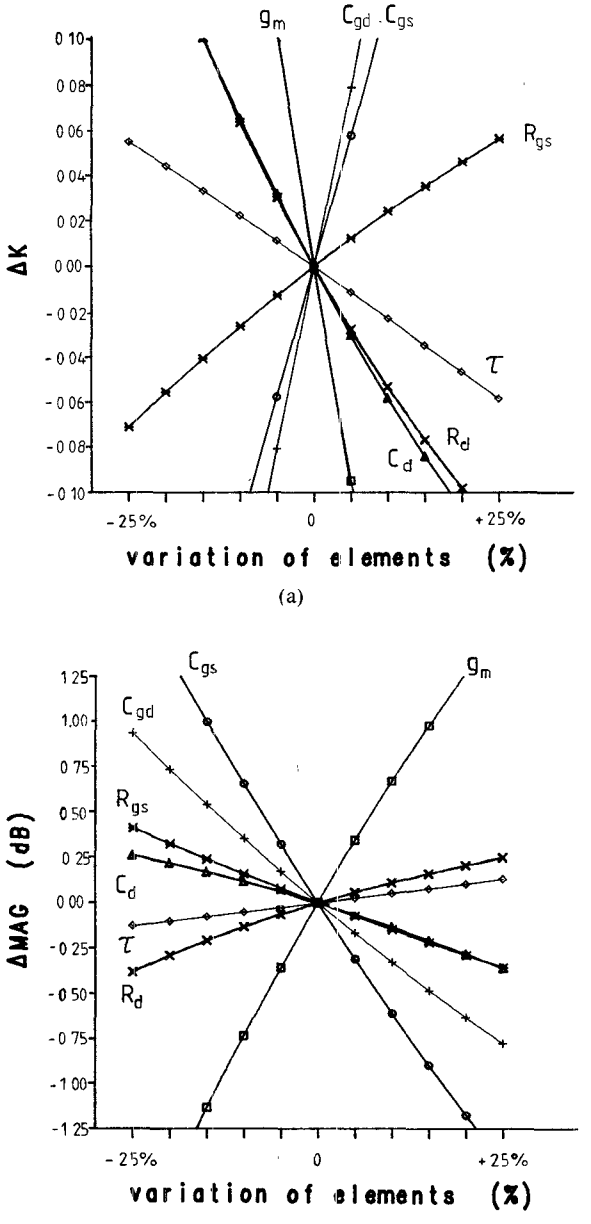


Fig. 7. Dependence of (a) stability factor, *K*, and (b) maximum available gain, *MAG*, on relative changes of elements of the equivalent circuit in Fig. 5 ($f = 10$ GHz).

are calculated from a simplified circuit without consideration of the parasitics C_{in}, C_{out}, L_D, L_S, and L_G but with the same intrinsic elements as shown in Fig. 5 (curve *b* in Fig. 6). The package introduces a strong increase of the phase shifts of S_{11} and S_{22} compared to measurements without the parasitics, as can be realized for example by wafer probing. Also, there is a remarkable influence on the magnitude and phase curve of the forward transmission S_{21} while only a small difference of S_{12} with and without parasitics can be observed.

These parasitic elements may reduce the stability factor *K*. If the FET works unstably no maximum available gain (*MAG*) can be calculated because this quantity is defined for $K \geq 1$ only. Therefore it is also necessary to know how intrinsic elements affect the high-frequency performance.

The dependence of the stability factor K and MAG on each element was analyzed by varying the values of the different elements in Fig. 5 one after another by ± 25 percent (Fig. 7). As expected, the lower g_m, C_d, and R_d and the higher C_{gs} and C_{gd}, the stronger the increase of the stability factor. On the other hand, the MAG is simultaneously reduced by the same elements.

V. Results and Discussion

At 300 K both the conventional and the superlattice HFET exhibit similar high-frequency performance (curve a in Figs. 8 and 9). This demonstrates that it is possible to design a superlattice HFET in such a way that it has nearly the same electrical properties as a conventional HFET at room temperature.

Cooling down the AlGaAs/GaAs HFET leads to the $I-V$ collapse mentioned above. The pronounced threshold voltage shift is due to the influence of deep traps in the AlGaAs layer. Consequently a significant decrease of the forward transmission curve (curve b in Fig. 8) relative to room-temperature values is found. Simultaneously the phase shift of S_{11} increases due to a larger gate–source capacitance while the magnitude of the output reflection coefficient S_{22} decreases, which corresponds to an increase of output conductance. The physical meaning as well as the bias dependence of the significant elements will be discussed later. Through illumination the influence of the DX-center is reduced and the HFET exhibits the expected performance (curve c in Fig. 8). Due to the strong increase of mobility and consequently the transconductance, the low-frequency forward transmission S_{21} with light is about four times higher than the room-temperature value. Also, the deterioration of the saturation behavior is reduced, which is indicated by a large output reflection coefficient S_{22}. Only the backward transmission S_{12} is nearly independent of temperature and light.

Replacing the homogeneously doped AlGaAs layer with a AlAs/GaAs superlattice leads to a much better high-frequency performance in the dark as compared to the conventional HFET (curve b in Fig. 9). While the input reflection coefficient S_{11} is only weakly dependent on temperature and light, the forward transmission S_{21} increases due to the higher mobility both in the dark and with illumination. The absolute value is lower than that of the conventional HFET because mobility and sheet carrier concentration at 120 K with illumination are slightly smaller than in the conventional HFET. The output resistance and consequently the S_{22} magnitude rise in the dark while illumination causes a reduction of this parameter. Simultaneously the backward transmission S_{12} decreases in the dark and therefore the maximum stable gain (MSG, ratio of S_{21} to S_{12}) is higher than the MSG of the illuminated sample. But the reduction of internal feedback combined with an increase of S_{22} magnitude causes a pronounced decrease of stability factor K, as will be shown later.

Next the method described in Section IV is now applied to extract the equivalent circuit from the S parameters

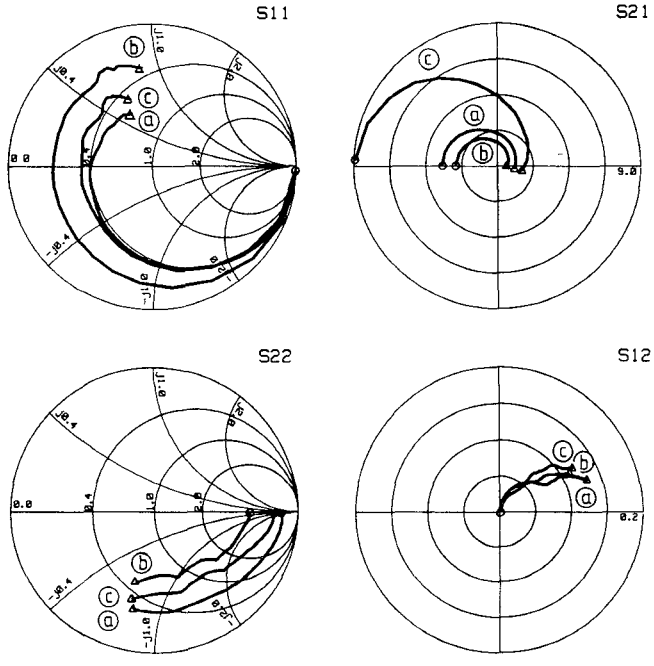


Fig. 8. Measured S parameters of the conventional n-AlGaAs/GaAs HFET at $V_{DS} = 2.5$ V, $V_{GS} = 0.5$ V. a: 300 K; b: 120 K (dark); c: 120 K (illuminated); ∘: 45 MHz; Δ: 10 GHz.

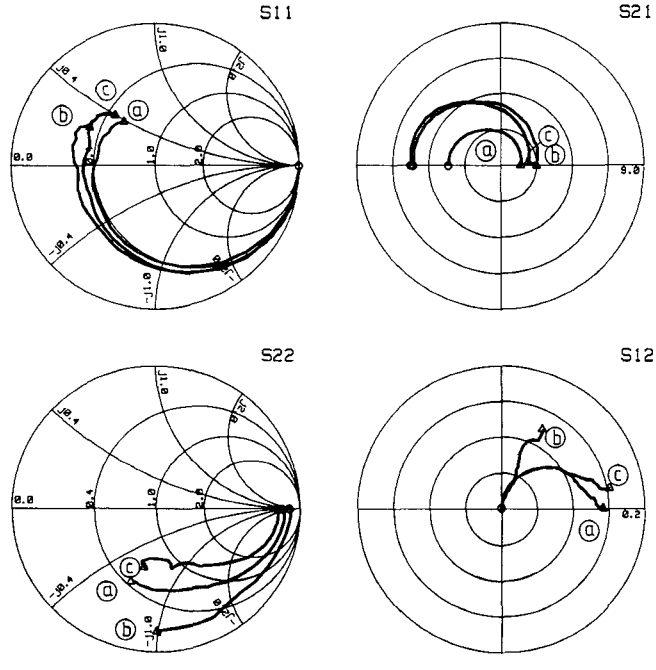


Fig. 9. Measured S parameters of the AlAs/GaAs SLHFET at $V_{DS} = 2.5$ V, $V_{GS} = 0.5$ V. a: 300 K; b: 120 K (dark); c: 120 K (illuminated); ∘: 45 MHz; Δ: 10 GHz.

discussed above. The main elements which dominate the RF performance are g_m, C_{gs}, and R_d. Their dependencies on gate–source voltage in the saturation region are investigated in detail. The transconductances of both types at 300 K are nearly the same (Fig. 10). But the DX-center in the AlGaAs layer causes carrier freeze-out and transconductance degradation at low temperatures in the dark combined with a significant threshold voltage shift and a

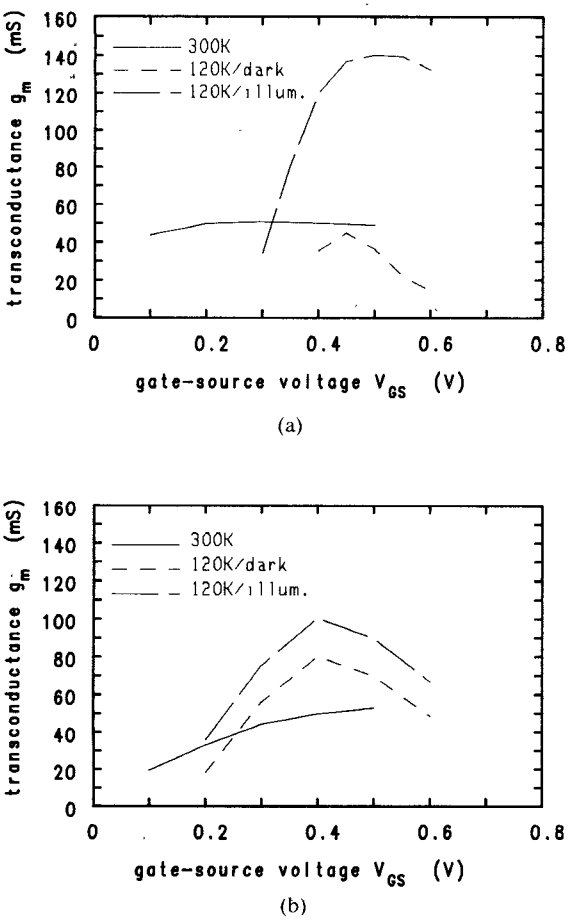


Fig. 10. Intrinsic transconductance g_m of (a) conventional AlGaAs/GaAs HFET and (b) AlAs/GaAs SLHFET as a function of V_{GS}.

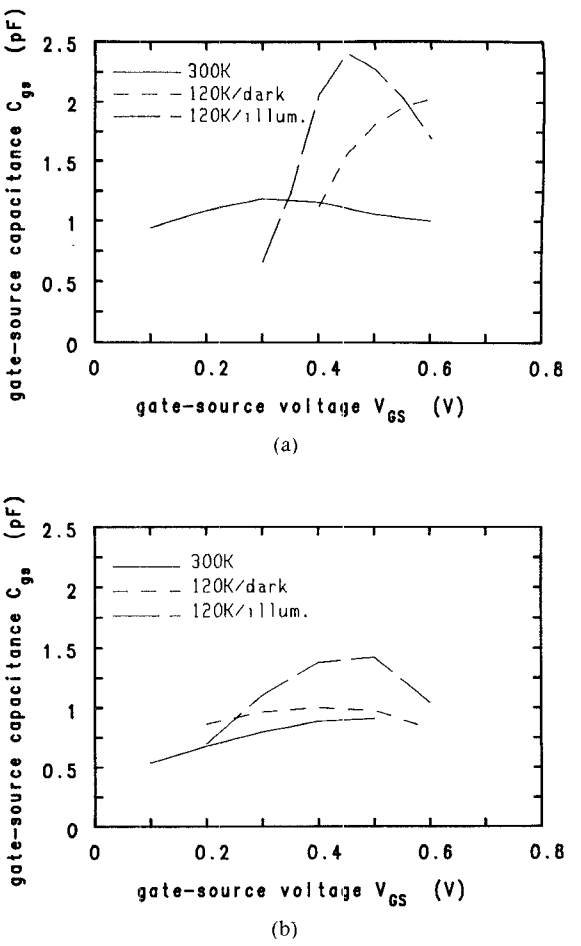


Fig. 11. Gate-source capacitance C_{gs} of (a) conventional AlGaAs/GaAs HFET and (b) AlAs/GaAs SLHFET as a function of V_{GS}.

compression of the usable bias range. The transconductance at 120 K in the dark is even lower than at room temperature. Under illumination deep donors are activated and a high transconductance can be achieved, as expected from improved low-temperature transport. The SLHFET exhibits a transconductance enhancement both in the dark and under illumination, indicating a strong reduction of the DX-center. But this enhancement is lower than that of the conventional structure because the carrier concentration in this structure is a little smaller.

The heterostructure FET is a charge-controlled device. Therefore transconductance and capacitance are directly coupled. The gate–source capacitance demonstrates a bias dependence similar to that of the transconductance (Fig. 11). Due to the higher carrier concentration at 120 K with light, the increase of C_{gs} of the AlGaAs/GaAs HFET is higher than that of the SLHFET while the values at room temperature are similar.

Fig. 12 demonstrates the temperature and light dependence of the output resistance for both the conventional and the superlattice structure. At 300 K the values of R_d are comparable. Combined with the collapse of the I–V characteristic at low temperatures in the dark, the saturation behavior of the n-AlGaAs/GaAs HFET deteriorates and leads to a reduced output resistance R_d. In the case of the superlattice structure R_d at 120 K in the dark is much higher but decreases with illumination. The reason for this behavior is not yet clear. The buffer below the 2DEG significantly dominates the saturation behavior of the FET's. Therefore the dependence on light of R_d may be explained by the light sensitivity of this buffer layer. This effect may also explain the light dependence of the backward transmission S_{12} represented by the gate–drain capacitance C_{gd} which is influenced by buffer effects as well.

The resulting MAG and the stability factor K of the conventional structure as a function of frequency at 300 K and at 120 K with and without illumination are shown in Fig. 13. The increase of transconductance at 120 K with illumination leads to an improvement in MAG of 2–3 dB but simultaneously the stability factor of the device is reduced.

For analog applications a high gain in a large range of bias voltage V_{GS} is necessary. Therefore comparison of gain values for one bias point only may be deceiving. In Fig. 14 the MAG's of both the AlGaAs/GaAs and the AlAs/GaAs HFET at 8 GHz and $V_{DS} = 2.5$ V are demonstrated. Due to the large threshold voltage shift in the conventional heterostructure, there is only a small bias range in which the FET exhibits a high power gain. Without illumination no significant gain can be achieved. If threshold voltage shift and I–V collapse are avoided, as in

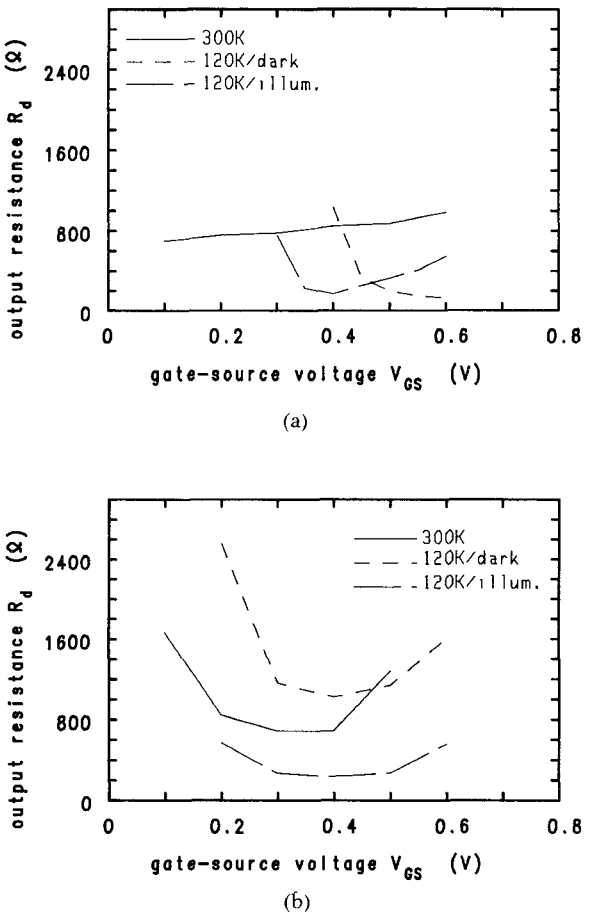


Fig. 12. Output resistance R_d of (a) conventional AlGaAs/GaAs HFET and (b) AlAs/GaAs SLHFET as a function of V_{GS}.

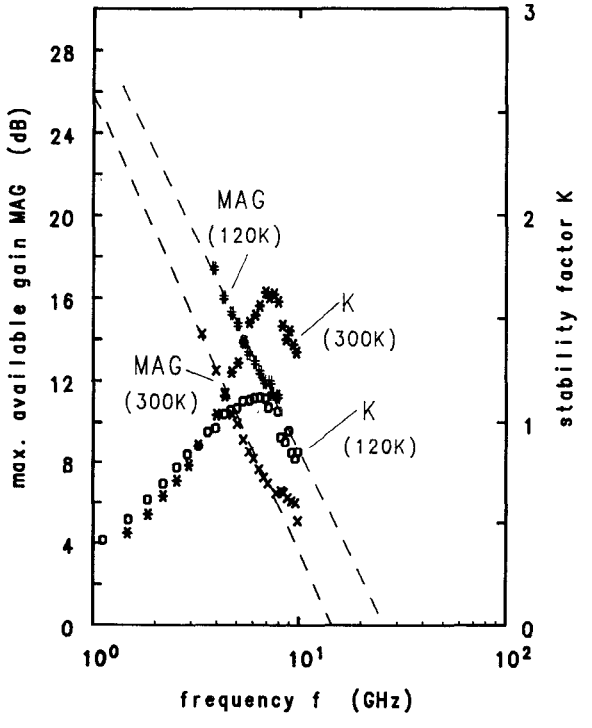


Fig. 13. Maximum available gain, *MAG*, and stability factor, *K*, of the conventional n-AlGaAs/GaAs HFET at $V_{DS} = 2.5$ V, $V_{GS} = 0.5$ V. ×: *MAG* (300 K); #: *MAG* (120 K/ill.); ∗: *K* (300 K); ∘: *K* (120 K/ill.).

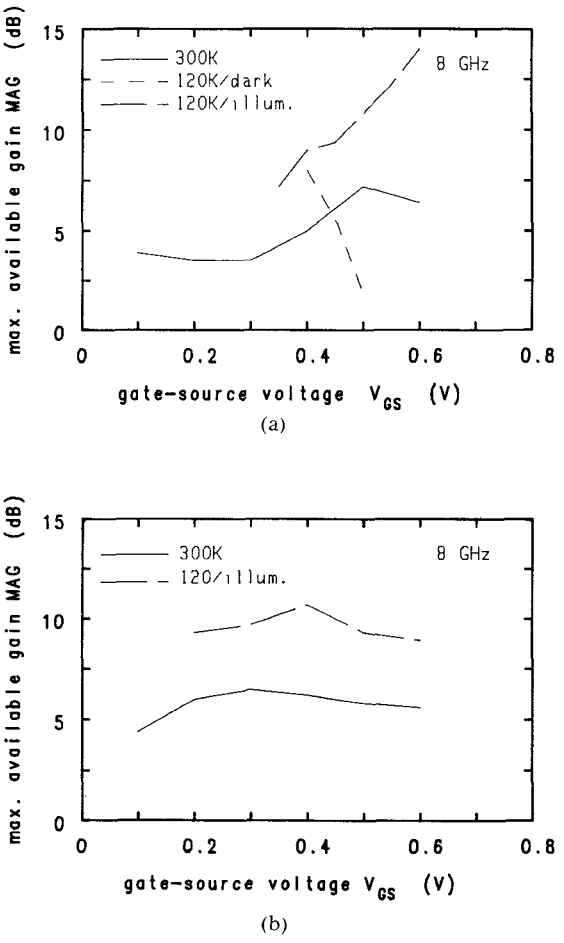


Fig. 14. Maximum available gain, *MAG*, of (a) conventional AlGaAs/GaAs HFET and (b) AlAs/GaAs SLHFET as a function of V_{GS} ($f = 8$ GHz).

the case of the SLHFET, a pronounced increase in *MAG* can be observed. But due to the large output resistance of the superlattice structure at 120 K in the dark combined with the decrease of internal feedback S_{12} and C_{gd}, the stability factor is less than unity and therefore no *MAG* can be determined without illumination. But it can be seen that it is possible to use the SLHFET at low temperatures in a wide bias range without deterioration of RF performance. Further investigations of the temperature dependence of the noise performance of these FET's will be carried out.

VI. Conclusion

A measurement setup for RF investigations at 120 K up to 12 GHz was presented for the first time. The method to extract the equivalent circuit from measured *S* parameters including parasitics was described. The influence of the transistor package, which is necessary for low-temperature RF measurements, was analyzed and the parameters for the intrinsic FET were evaluated.

A comprehensive study of the high-frequency performance of heterostructure FET's at low temperatures was presented. The differences between a superlattice and a conventional AlGaAs/GaAs HFET with a high Al content were investigated in detail by an analysis of the bias and

temperature dependence of the elements of the equivalent circuit. The advantage of the superlattice over of a homogeneously doped AlGaAs layer with a high effective Al content and simultaneously a remarkably improved RF performance at low temperatures both in the dark and with illumination was demonstrated.

Although the gate lengths of the investigated HFET's are greater than 1 μm, the described method as well as the results of this analysis can be transferred to submicron devices without any restrictions. Therefore submicron superlattice HFET's may exhibit high power gain at 300 K as well as at lower temperatures both in the dark and under illumination.

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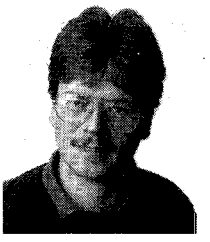

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